KE12LS200T SIC CLD LTSPICE MODEL

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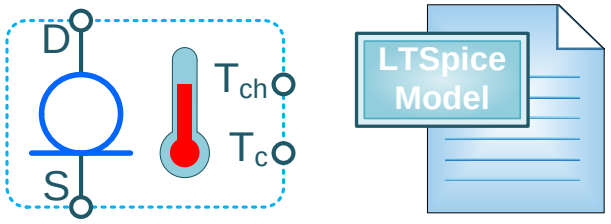
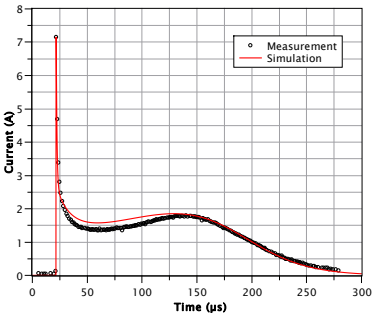
ABSTRACT

This application note describes the derivation and how to use SiC CLD electro-thermal LTSpice model. This covers 1.2kV / 2 Ohm SiC Current Limiting Device (CLD) KE12LS200T for lightning protection applications. This application note first describes the model, then provides instructions on how to import the model into LTSpice, and finally compares test and simulations results.



SiC CLD LTSpice symbol



Experimental vs Simulation waveforms

This Application Note is aimed at customers designing and deploying SiC CLD-based lightning and surge protection applications, by helping them to integrate the proposed SiC CLD model into LTSpice in order to perform device and system-level simulations.

SIC CURRENT LIMITING DEVICE MODELING PROCEDURE

To derive the SiC CLD models, state-of-the-art Finite Element Analysis tools have been used. Derived models have been adapted in order to ease integration into LTSpice. Extensive verification and validation has been carried out though multiple system-level simulations in different environments as well as through experimental measurements. The device modeling procedure is presented in Figure 1.

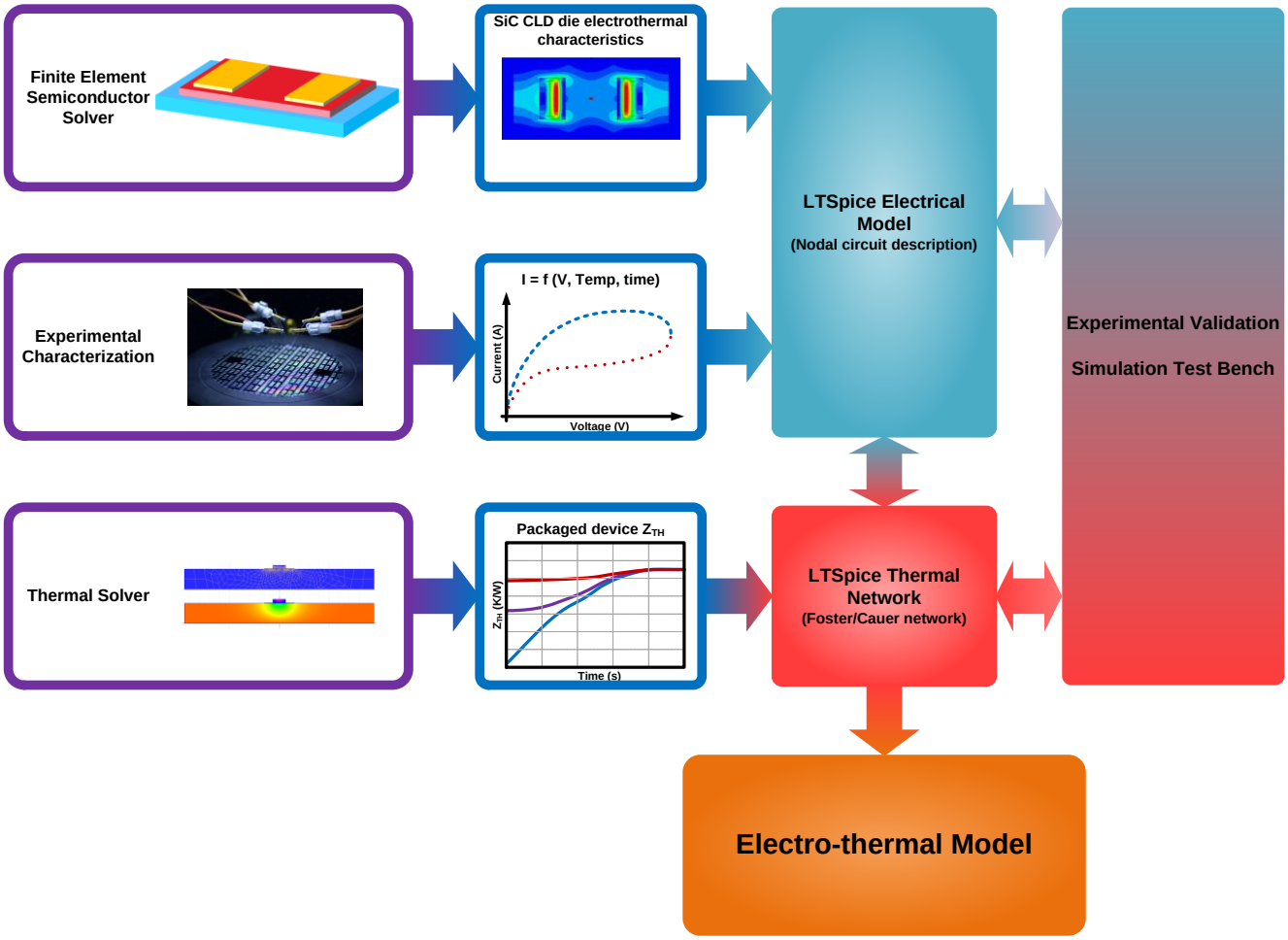


Figure 1. Device modeling procedure.

CURRENT LIMITING DEVICE LTSPICE MODEL DESCRIPTION

Physical parameters such as the electron mobility, playing an important role in the behavior of semiconductor devices, are strongly dependent upon temperature. However, very few SPICE-like models properly consider the impact of temperature on these physical parameters. That is why many semiconductor device models are so inaccurate. In fact, temperature effects in widespread SPICE models are, at best, partially implemented. Indeed, lattice temperature is often introduced as an optional fixed parameter that the user can set only once before launching a simulation.

In general, neglecting temperature effects brings quite good simulation results in low power applications since the devices run in quasi-isothermal conditions. Feedback and/or error correction in complex circuits also help to compensate for thermal drifts.

However, in power applications, considerable amounts of power can be dissipated in the devices leading to important die temperature variations. In this case, the temperature must be considered as a dynamic parameter along with voltages and currents. To provide accurate results, the dynamic aspect of the temperature must be implemented in SPICE models. Such a model is said electro-thermal.

Aside from improving the simulation accuracy, electro-thermal modeling allows monitoring the device temperature (generally the junction or channel temperature) and helps to prevent thermal failures due to excessive dissipated power.

Regarding the CLD, this information is of prime importance since it enables to dimension precisely the protection circuit and thus ensure the best reliability.

As all SPICE-like models, its validity domain is restricted and careful attention must be paid on results especially at extreme values of voltage and/or temperature. That's why a complete validation of the model must be performed under relevant electrical stimuli, as shown in the next section.

Figure 2 shows the diagram of the sub-circuit used in the CLD electro-thermal model. It consists of an electrical description of the CLD based on lumped elements coupled with a thermal model for both the die and the package.

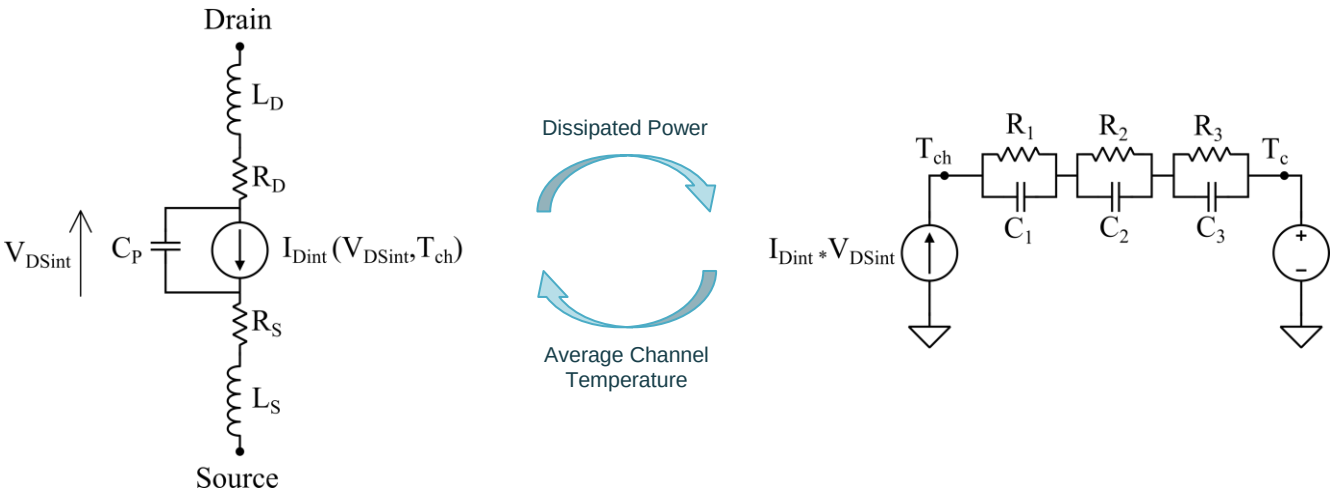


Figure 2: CLD electro-thermal model circuit diagram

The electrical description includes linear (parasitic resistors, inductors and capacitors) and nonlinear devices (intrinsic current source), thus describing the forward and reverse behavior of the CLD through intrinsic parameters (V_{DSint}, I_{Dint}) and parasitic elements (C_P) of the device. Parasitic packaging and extrinsic access elements are also included (L_D, L_S, R_D, R_S). In Figure 2, T_{ch} represents the average channel temperature whereas T_c is the average case temperature.

Appropriate electrical characterization is the keystone for accurate modeling. To ensure accuracy, electrical characterization must be performed using ultra-fast pulsed-IV measurements to avoid self-heating, and this over a wide temperature span (typically -50°C to 200°C). That way, it is then possible to identify the thermal parame-

ters of the device and build a set of descriptive equations for the device behavior. An example is shown in Figure 3.

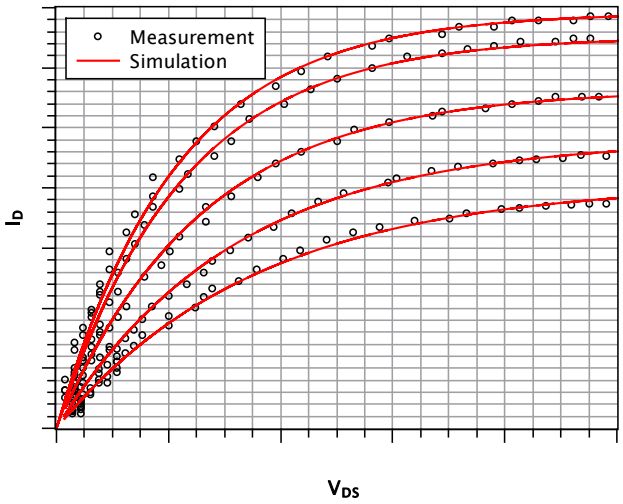
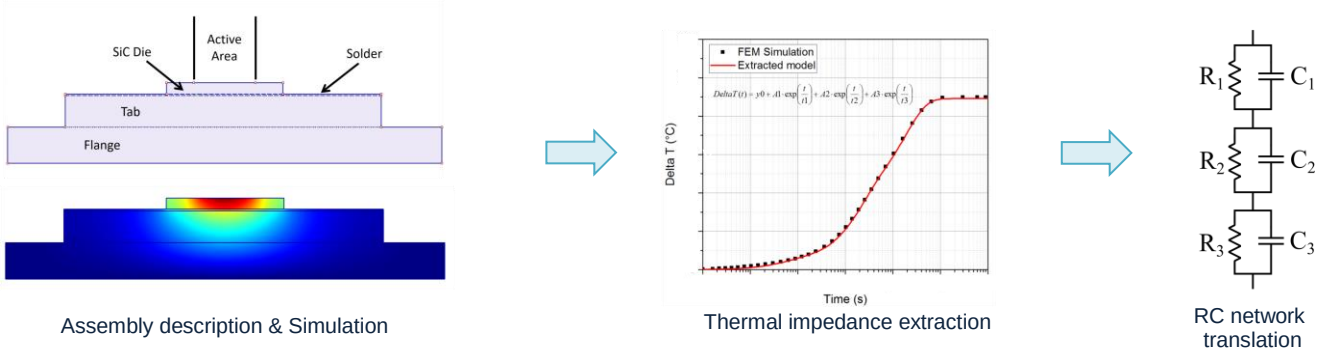


Figure 3: Isothermal CLD IV curves for different temperatures

Aside the electrical characterization, the thermal description of the die+package assembly is carried out through finite element method (FEM) simulations. The thermal impulse response (i.e. thermal impedance) of the structure is extracted and represented as an electrical RC network (Figure 4) which enables steady-state and transient self-heating prediction.



Assembly description & Simulation

Thermal impedance extraction

RC network translation

Figure 4: Thermal impedance extraction

Both parts of the model are then coupled in a compact SPICE model to be used in LTSpice. The power dissipated by the junction is calculated, fed into the thermal RC network and turned into a temperature rise. New voltages and currents are then calculated with this temperature. This sequence repeats at every simulation step, giving realistic instantaneous voltages, currents and junction temperatures.

MEASUREMENTS AND SIMULATION RESULTS

This section illustrates the usage of this electro-thermal model into the LTSpice environment. To get started with the CLD electro-thermal model on LTSpice, please refer to the next section.

The CLD symbol is picked up from the library and connected to the model of a surge waveform generator. Figure 5 depicts the LTSpice schematic. “D” and “S” are respectively input and output terminals. Voltage on terminal “Tch” corresponds to the average channel temperature whereas “Tc” provides the case temperature. The latter can be set by changing the Tc parameter (20°C is the default value) of the CLD model.

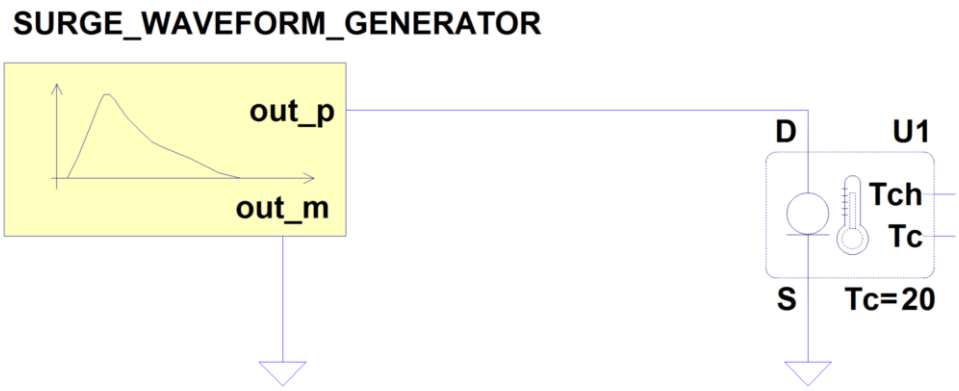


Figure 5: LTSpice sheet with CLD

The following curves compare measurements and simulations when the KE12LS200T CLD is struck by a 1.2/50µs voltage waveform (2 ohms generator impedance). Waveforms with 175V and 900V peak voltage are considered in Figure 6 and Figure 7 respectively to show different power levels and estimated junction temperatures. Measurements and simulations were performed at 20°C ambient temperature.

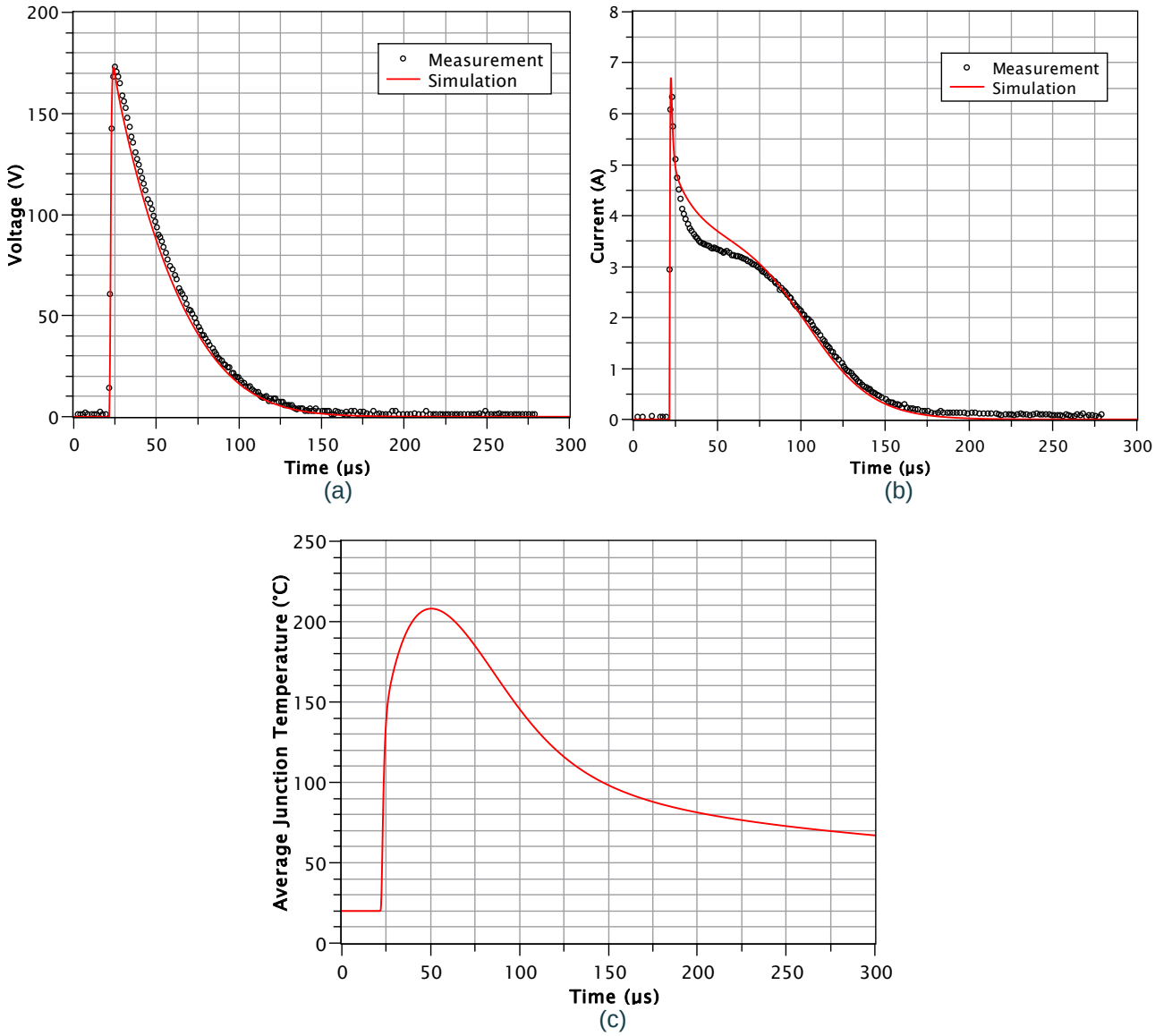


Figure 6: Measured and simulated responses to a 175V 1.2/50µs waveform: (a) Input waveform. (b) Current through CLD. (c) Simulated temperature

Table 1. Comparison of SiC CLD response to a 175V 1.2/50µs waveform.

Electrical characteristics	Measurement	Simulation	Difference (%)
Peak current I_{MAX} (A)	6,6 A	6,7 A	1,5 %
Peak voltage V_{MAX} (V)	173 V	172 V	-0,6 %
Energy E_{CLD} (mJ)	23.3 mJ	23.1 mJ	-0.9 %
Maximal channel temperature (°C)	-	208 °C	-

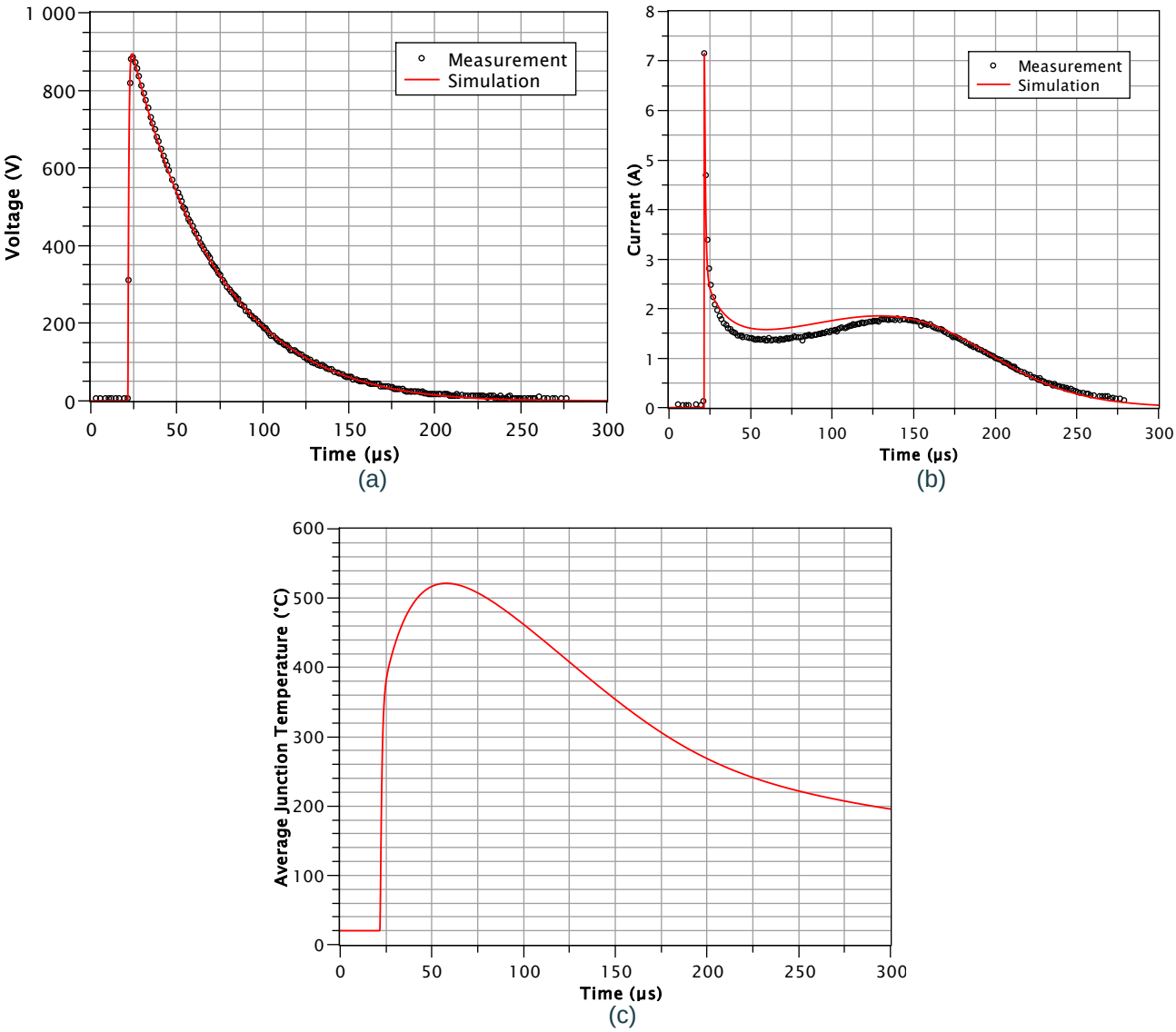


Figure 7: Measured and simulated responses to a 900V 1.2/50µs waveform: (a) Input waveform. (b) Current through CLD. (c) Simulated temperature

Table 2. Comparison of SiC CLD response to a 900V 1.2/50µs waveform.

Electrical characteristics	Measurement	Simulation	Difference (%)
Peak current I_{MAX} (A)	7.1 A	7.1 A	0 %
Peak voltage V_{MAX} (V)	887 V	895 V	0,9 %
Energy E_{CLD} (mJ)	77.3 mJ	82.1 mJ	5.8 %
Maximal channel temperature (°C)	-	521 °C	-

We can notice very good agreement between measurements and simulations even at high dissipated power levels, i.e. high channel temperatures.

IMPORTING THE SIC CLD MODEL INTO LTSPICE

The LTSpice model of the KE12LS200T (TO-247 package) SiC CLD is available with its symbol from the web-site of CALY Technologies. The model description comes as an encrypted text file readable by LTSpice (Figure 8). Any modification of the file header or its contents would make the model unreadable by LTSpice.

```
* LTspice Encrypted File
* This model is the property of CALY Technologies.
* This encrypted file has been supplied by a 3rd
* party vendor that does not wish to publicize
* the technology used to implement this library.
*
* Permission is granted to use this file for
* simulations but not to reverse engineer its
* contents.
* This file is provided as is, where is.
*
************************************************
*
* SiC Current Limiter Electrothermal Spice Model KE12LS200T v1.1
* Copyright 2017 CALY Technologies
* Author: Jean-Baptiste FONDER
* Email : j.fonder@caly-technologies.com
*
* This is an empirical model of KE12LS200T unidirectional SiC current limiter based on typical characteristics of the device as shown in the datasheet.
* It is not warranted by CALY Technologies as fully representing all of the specifications and operating characteristics of the device.
* This model includes self heating effects.
* Its accuracy is best in the the range of -50C to 200C but can be used to extrapolate characteristics up to 650C.
* Drain to Source breakdown as well as reverse conduction are notional only.
*
* SYMBOL LAYOUT :
* - D pin, current input (Anode)
* - S pin, current output (Cathode)
* - Tch pin, channel temperature (Tj)
* - Tc pin, case temperature (Tcase)
*
* REMARKS :
* Default Tc value is 20C, though it can be changed.
* To disable self heating effects and fix Tch temperature, just short Tc to Tch and specify the desired Tc.
*
************************************************
*
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Figure 8. KE12LS200T SiC CLD model header file. (LTSpice encrypted model): "KE12LS200T.txt"

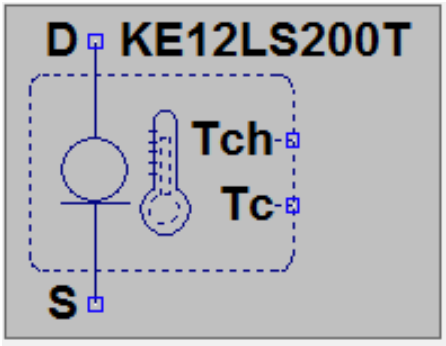
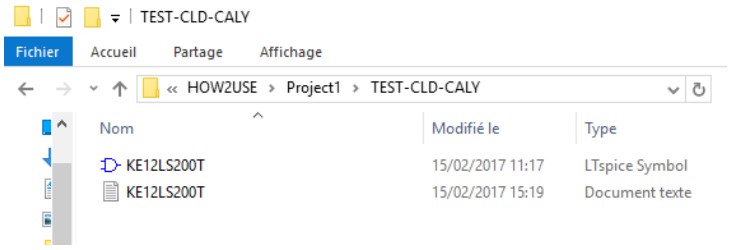
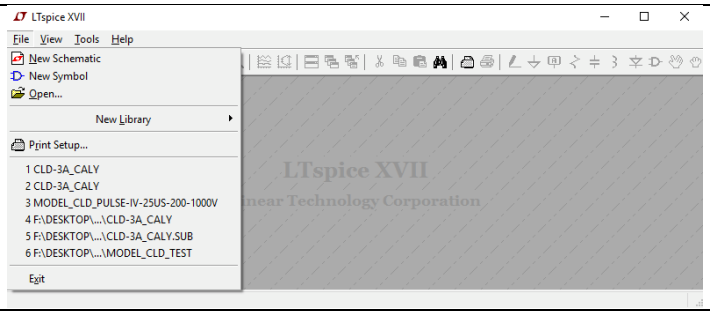
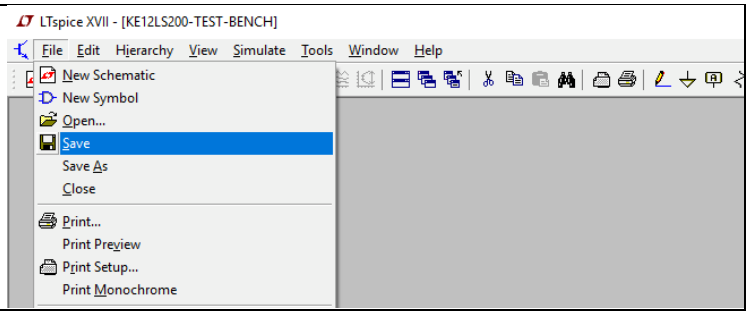
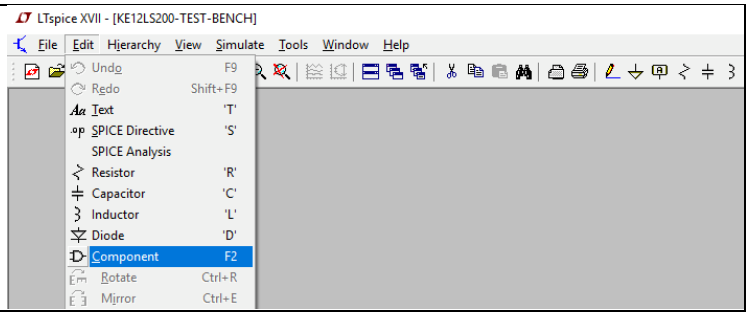
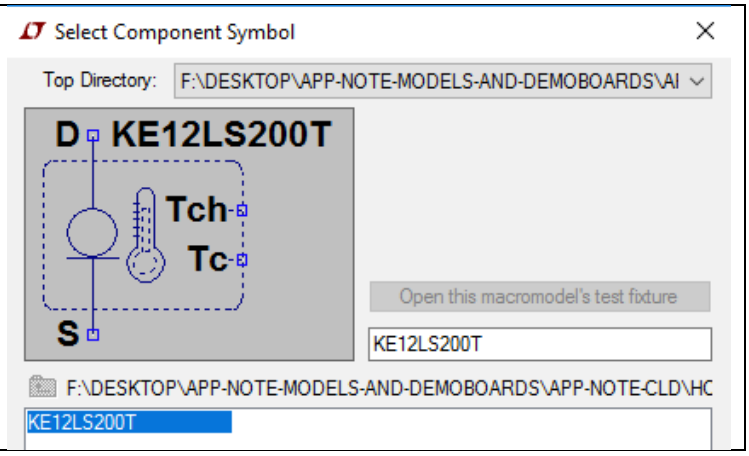
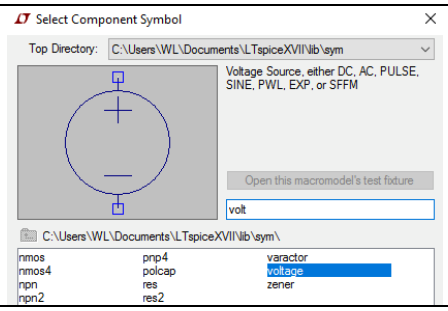
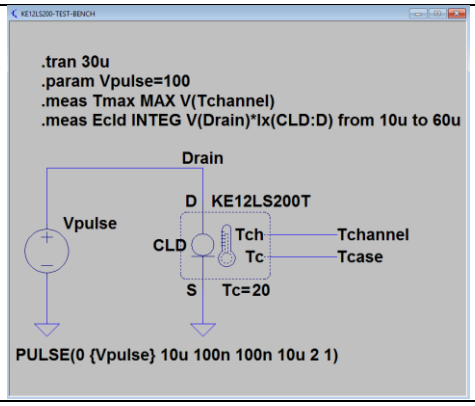
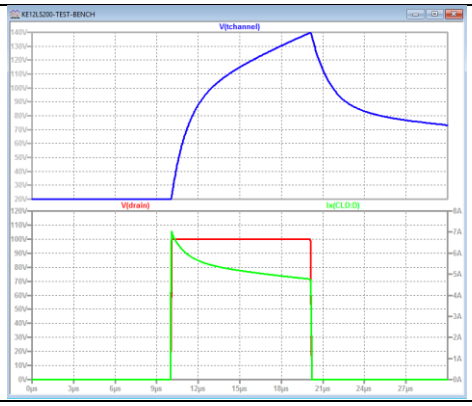


Figure 9. KE12LS200T SiC CLD symbol file: "KE12LS200T.asy"

Using the model from a custom folder.

STEP	ACTION	SCREEN CAPTURE
1	Create a project folder **"TEST-CLD-CALY"** Add the SiC CLD model files **KE12LS200T.txt** and **KE12LS200T.asy** to this project folder	
2	LAUNCH LTSpice software	
3	Create a blank schematic	
4	Save Schematic to project folder "KE12LS200-TEST-BENCH.asc"	
5	Place a new component onto the schematic "F2 function Key"	

6	The “Select Component Symbol” window opens. B) Change “Top Directory” to the Project folder C) Pick-up **KE12LS200T** symbol and place it onto the simulation sheet.	
7	Add voltage source A) “F2 function Key” B) Change “Top Directory” to the LTspice Symbols folder C) Select and place voltage source	
8	A) Place GND and wires to connect Voltage source and CLD as illustrated in the screen capture. B) Define voltage source parameters as well as spice simulation directives	
9	Launch the simulation (Simulate -> Run) and add parameters to the plot window	

In this example, the CLD is subjected to a 100V square pulse. Self-heating is calculated and the simulated temperature increases up to 139 °C. The dissipated energy value is E_{CLD} = 5.3 mJo.
The user can investigate several advantages of SiC CLD in its own application and evaluate:

- Fast transient self-heating modeling
- Peak current and thermal effect prediction
- Maximal channel temperature estimation

REVISION HISTORY

Revision	Date	Description
1A	2017-Mar-15	First issue
1B	2017-Apr-24	Amended typo in Table of Contents title.
1C	2018-Aug-09	Amended links in Contact Us Section

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